90 Rec'd PCT/PTO 03 MAY 2001

Form PTO-1390	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER P20914
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/807993

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00046	5 January 2000	15 January 1999

TITLE OF INVENTION

CIRCUIT ARRANGEMENT FOR FORMING THE TERMINATION OF AN ANALOG SUBSCRIBER LINE

APPLICANT(S) FOR DO/EO/US

Joerg HAUPTMANN and Alexander KAHL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. _X_ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ___ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. _X_ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. _X_ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. _X_ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 a. _X_ is attached hereto (required only if not communicated by the International Bureau).
 b. ___ has been communicated by the International Bureau.
 c. ___ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. _X_ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
7. ___ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 a. ___ are attached hereto (required only if not communicated by the International Bureau).
 b. ___ have been communicated by the International Bureau.
 c. ___ have not been made; however, the time limit for making such amendments has NOT expired.
 d. ___ have not been made and will not be made.
8. ___ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3))
9. _X_ An oath or declaration of the inventor(s) (35 U.S.C. .371(c)(4)).
 "Unexecuted"
10. ___ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (U.S.C. 371(c)(5)).

Items 11 to 16 below concern other document(s) or information included:

11. Assignee: INFINEON TECHNOLOGIES AG of München, GERMANY
12. ___ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
13. ___ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
14. _X_ A FIRST preliminary amendment.
 ___ A SECOND or SUBSEQUENT preliminary amendment.
15. ___ A substitute specification.
16. ___ A change of power of attorney and/or address letter.
17. ___ Figure of Drawing to be published_____
18. _X_ Other items or information:
 Cover Sheet and International Application as published in German.
 PCT/IPEA/416(in German).
 PCT/IPEA/409(in German).
 PCT/ISA/210(in English and German).
 Cover Letter under 35 USC 371 and 1.495.
 Claim of Priority.

JC18 Rec'd PCT/PTO 03 MAY 2001

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/807993	PCT/DE00/00046	P20914

19. ___ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Search report has been prepared by the EPO or JPO. $ 860.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482). $ 690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO(37 CFR 1.445(a)(2). $ 710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO. $1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4). $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ___ 20 ___ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	RATE		
Total Claims	5 - 20 =	0	X $18.00	$0.00	
Independent Claims	1 - 3 =	0	X $80.00	$0.00	
Multiple dependent claim(s) (if applicable)			+ $270.00	$0.00	
			TOTAL OF ABOVE CALCULATIONS =	$860.00	
___ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$	
			SUBTOTAL =	$860.00	
Processing fee of $130.00 for furnishing the English translation later than ___ 20 ___ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +					
Extension of Time fee in the amount of $					
			TOTAL NATIONAL FEE =	$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +					
			TOTAL FEES ENCLOSED =	$860.00	
			Amount to be refunded	$	
			Charged	$	

a. _X_ A check in the amount of $860.00 to cover the above fees is enclosed.

b. ___ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees.

c. _X_ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-0089.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO **CUSTOMER NO. 7055**
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NAME

29,027
REGISTRATION NUMBER

09/807993
JC18 Rec'd PCT/PTO 03 MAY 2001

P20914.A01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : J. HAUPTMANN et al.

Serial No : Not Yet Assigned (National Stage of PCT/DE00/00046)

Filed : Concurrently Herewith (International Filing Date January 5, 2000)

For : CIRCUIT ARRANGEMENT FOR FORMING THE TERMINATION OF AN ANALOG SUBSCRIBER LINE

PRELIMINARY AMENDMENT

10/019359
PCT/DE00/00046

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to calculation of the filing fees and the examination of the above-identified patent application on the merits, the Examiner is respectfully requested to amend the claims as follows:

IN THE CLAIMS

Please amend claims 1-4 as follows (a marked-up copy of the claim amendments is provided as an attachment to this Amendment):

1. (Amended-Clean Text) A circuit arrangement for forming the termination of an analog subscriber line which has a first connection and a second connection for the subscriber line, and where the first connection is connected to the second connection by a

series circuit comprising a first capacitor, at least one variable resistor and a second capacitor, a DC source being connected to the node point between the first capacitor and the variable resistor.

2. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein the DC source has a transistor and a resistor, the load path of the transistor being connected in series with the resistor, and the control connection of the transistor being set by a control circuit.

3. (Amended-Clean Text) The circuit arrangement as claimed in claim 2, wherein the control circuit has an operational amplifier whose output is connected to the control connection of the transistor of the DC source, whose negative input is connected to the junction point between the transistor and the resistor of the DC source and whose positive input has a reference voltage applied to it.

4. (Amended-Clean Text) The circuit arrangement as claimed in claim 2 wherein the DC source has a diode which is connected in series with the load path of the transistor.

Please add new claim 5 as follows:

---5. The circuit arrangement as claimed in claim 3 wherein the DC source has a diode which is connected in series with the load path of the transistor.---

REMARKS

By the above amendment, claims 1-4 have been amended and claim 5 has been added so as to be placed in accepted U.S. format and to delete reference symbols and multiple dependency.

If there should be any questions, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
J. HAUPTMANN et al.

Leslie J. Paperner Reg No. 33,329
Bruce H. Bernstein
Reg. No. 29,027

May 2, 2001
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P20914.A01

MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A circuit arrangement for forming the termination of an analog subscriber line which has a first connection [(a)] and a second connection [(b)] for the subscriber line, and where the first connection [(a)] is connected to the second connection [(b)] by [means of] a series circuit comprising a first capacitor [(C1)], at least one variable resistor [(T1, R1, T2, R2)] and a second capacitor [(C2)], a DC source [(T3, R5, VDDA)] being connected to the node point [(1)] between the first capacitor [(C1)] and the variable resistor [(T1, R1)].

2. (Amended) The circuit arrangement as claimed in claim 1, wherein [characterized in that]

the DC source [(T3, R5, VDDA)] has a transistor [(T3)] and a resistor [(R5)], the load path of the transistor being connected in series with the resistor, and the control connection of the transistor being set by a control circuit [(5)].

3. (Amended) The circuit arrangement as claimed in claim 2, wherein [characterized in that]

the control circuit has an operational amplifier [(5)] whose output is connected to the control connection of the transistor [(T3)] of the DC source, whose negative input is connected to

the junction point between the transistor [(T3)] and the resistor [(R5)] of the DC source and whose positive input has a reference voltage [(VREF)] applied to it.

4. (Amended) The circuit arrangement as claimed in claim 2 [or 3, characterized in that] wherein

the DC source has a diode [(D1)] which is connected in series with the load path of the transistor [(T3)].

Replacement Sheet

Description

Circuit arrangement for forming the termination of an analog subscriber line

The invention relates to a circuit arrangement for forming the termination of an analog subscriber line in accordance with the precharacterizing clause of patent claim 1.

A circuit arrangement for terminating an analog subscriber line (SLIC = Subscriber Line Circuit) at the subscriber end forms a terminal impedance for the subscriber line both for AC signals and for DC signals. In this context, the terminal impedance for DC signals (DC terminal impedance) and for AC signals (AC terminal impedance) is connected to the subscriber line when there is a connection for signal transmission.

The DC terminal impedance is used to set an operating point for the circuit arrangement for terminating the analog subscriber line and to signal to a remote station (e.g. an exchange) that there is a connection. When signals (e.g. voice or data signals) are transmitted or received, the current flowing through the subscriber line is then modulated by the operating point set by the DC terminal impedance. In this case, the operating point depends on the direct current, supplied by the remote station, which flows through the subscriber line and on the DC characteristic set by the DC terminal impedance.

The DC and AC terminal impedances can be changed or adjusted in line with country-specific requirements only by changing the circuitry, for example by replacing resistors, capacitors, etc.

The technical problem on which the invention is based is therefore that of specifying a circuit arrangement

for terminating an analog subscriber line which forms, with little circuit complexity, a controllable AC terminal impedance which is programmable, and where the subscriber line is free of direct current.

This problem is achieved by a circuit arrangement having the features of patent claim 1. Advantageous embodiments of the invention can be found in the respective dependent claims.

The invention relates to a circuit arrangement for forming the termination of an analog subscriber line which has a first connection and a second connection for connecting the two-wire analog subscriber line. The first connection is connected to the second connection by means of a series circuit comprising a first capacitor, at least one variable resistor and a second capacitor. According to the invention, a DC source is connected to the junction point between the first capacitor and the variable resistor. The DC source impresses a current which is used to set an operating point for signal transmission via the analog subscriber line. The first and the second capacitor mean that DC signals are blocked on the subscriber line, so that no direct current can flow through the analog subscriber line. In addition, a terminal impedance for AC signals is formed by means of the first and the second capacitor and the variable resistors. The variable resistors allow the operating point to be set for DC signals and allow the terminal impedance to be set for AC signals.

In one preferred embodiment, the DC source is formed by a transistor and a resistor, the load path of the transistor being connected in series with the resistor, and the free connection of the resistor being connected to a supply voltage. The control connection of the transistor is connected to the junction point between

the load path of the transistor and the resistor by means of a control circuit.

In a particularly preferred embodiment, the control circuit for the DC source has an operational amplifier which compares the voltage at the junction point between the load path of the transistor and the resistor with a reference voltage and uses its output voltage to control the transistor on the basis of this.

Preferably, the DC source has a diode which is connected in series with the load path of the transistor. Advantageously, the diode prevents the transistor from becoming damaged by the high voltages of a call signal.

Other advantages, features and opportunities for application of the invention can be found in the description of illustrative embodiments below in conjunction with the drawing. In the drawing:

Figure 1 shows an illustrative embodiment of the circuit arrangement for terminating an analog subscriber line which is used in a module for data transmission via an analog subscriber line.

Figure 1 shows a circuit arrangement for terminating an analog subscriber line, where the analog subscriber line has two wires which can be connected to a first connection a and to a second connection b of the circuit arrangement.

The first connection a is connected to a reference-ground potential VSS via a series circuit comprising a first capacitor C1, a first n-channel MOSFET T1 and a first resistor R1. The second connection b is connected to the reference-ground potential VSS via a series circuit comprising a second capacitor C2, a second n-

channel MOSFET T2 and a second resistor R2. In this illustrative embodiment, the reference-ground potential VSS is equal to the zero potential. The first capacitor C1 and the second capacitor C2 block DC signals on the analog subscriber line. Hence, no direct current flows into the circuit arrangement via the subscriber line.

To set a DC operating point for the circuit arrangement, a voltage is measured at the junction point 1 between the first capacitor and the first n-channel MOSFET T1 using a first voltage divider R3 and R6 and is supplied to a DC operating point control circuit 3. In addition, a voltage is measured at the junction point 11 between the second capacitor C2 and the second n-channel MOSFET T2 using a second voltage divider R4 and R7 and is supplied to the DC operating point control circuit 3. The DC operating point control circuit 3 uses an adding circuit 4 and an analog integrator circuit 2 to control the resistance of the load path of the first n-channel MOSFET T1, and hence the DC operating point of the circuit arrangement.

So that measurable DC voltages are produced at the junction point 1 and the junction point 11, the junction point 1 is connected to a DC source which impresses a current I. The control connection of the second n-channel MOSFET T2 is at a high potential VHIGH in this operating state, which means that the resistance of the load path of the second n-channel MOSFET T2 has a low value.

The DC source for impressing the current I has a pnp bipolar transistor T3, a resistor R5 and an operational amplifier 5. One end of the resistor R5 is connected to a supply voltage VDDA, and the other end is connected to the emitter of the pnp bipolar transistor T3. From the collector of the pnp bipolar transistor T3 flows the current I which is impressed into the circuit arrangement. The positive input of the operational

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amplifier 5 is supplied with a reference voltage VREF, and the negative input of the operational amplifier 5 is supplied with the voltage on the emitter of the pnp bipolar transistor T3. The output voltage from the operational amplifier 5 controls the pnp bipolar transistor T3. The collector of the pnp bipolar transistor also has the anode of a diode D1 connected to it. The diode D1 is used to protect the pnp bipolar transistor T3 against destruction by the high voltages of the call signals. The reference voltage VREF can be used to set the current I.

An AC terminal impedance for the analog subscriber line is set digitally by means of an impedance filter 8.

To this end, an AC voltage at the junction point 1 is supplied to the impedance filter 8 via a third capacitor C3 and an analog/digital converter 6 connected downstream. In addition, an AC voltage at the junction point 11 is supplied to the impedance filter 8 via a fourth capacitor C4 and a second analog/digital converter 9 connected downstream. The impedance filter 8, which may be in the form of a digital filter, uses the digital AC signals to calculate a signal required for setting the AC terminal impedance. The signal is converted into an analog voltage by means of a digital/analog converter 7 and is added to the output voltage of the circuit by the adding circuit 4 in order to set the DC operating point 3. The output voltage of the adding circuit 4 is supplied to the analog integrator circuit 2, which subtracts a voltage at the junction point between the n-channel MOSFET T1 and the first resistor R1 from the supplied voltage and integrates the difference voltage.

This circuit arrangement is provided with two different setting paths for setting both the DC operating point and the AC terminal impedance, with the first n-channel MOSFET T1 being used for setting the AC terminal

impedance and the DC operating point. Since a direct current or a DC voltage is blocked on the subscriber line by the first capacitor C1 and the second capacitor C2 in this circuit arrangement, the DC source needs to impress a current I through the first n-channel MOSFET T1, the first resistor R1, the second resistor R2 and the second n-channel MOSFET T2 in order to set the DC operating point. The DC operating point control circuit 3 and the first n-channel MOSFET T1 are then used to set the direct current through the load path of the first n-channel MOSFET T1, and hence the DC operating point.

ERSATZBLATT (REGEL 26)

Patent Claims

1. A circuit arrangement for forming the termination of an analog subscriber line which has a first connection (a) and a second connection (b) for the subscriber line, and where the first connection (a) is connected to the second connection (b) by means of a series circuit comprising a first capacitor (C1), at least one variable resistor (T1, R1, T2, R2) and a second capacitor (C2), a DC source (T3, R5, VDDA) being connected to the node point (1) between the first capacitor (C1) and the variable resistor (T1, R1).

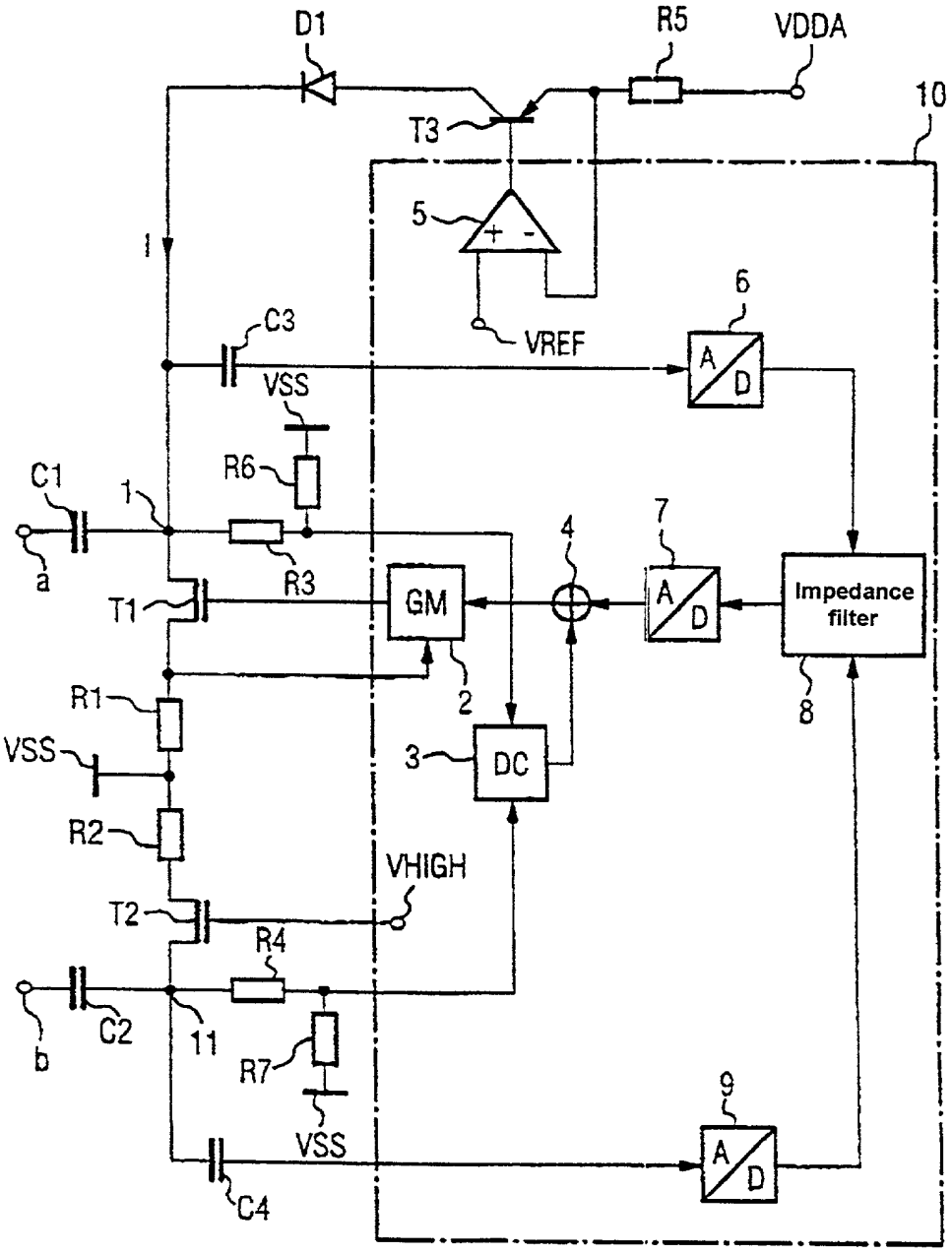
2. The circuit arrangement as claimed in claim 1, characterized in that
the DC source (T3, R5, VDDA) has a transistor (T3) and a resistor (R5), the load path of the transistor being connected in series with the resistor, and the control connection of the transistor being set by a control circuit (5).

3. The circuit arrangement as claimed in claim 2, characterized in that
the control circuit has an operational amplifier (5) whose output is connected to the control connection of the transistor (T3) of the DC source, whose negative input is connected to the junction point between the transistor (T3) and the resistor (R5) of the DC source and whose positive input has a reference voltage (VREF) applied to it.

4. The circuit arrangement as claimed in claim 2 or 3,
characterized in that
the DC source has a diode (D1) which is connected in series with the load path of the transistor (T3).

ERSATZBLATT (REGEL 26)

1/1


D1
R5
VDDA
10
T3
5
+
-
1
VREF
6
C3
A
D
VSS
R6
C1
1
a
R3
T1
GM
4
7
A
D
Impedance filter
2
8
R1
VSS
3
DC
R2
VHIGH
T2
R4
C2
11
b
R7
9
VSS
A
D
C4

Declaration and Pow[illegible]f Attorney For Utility or Design Pat[illegible] Application

Erklärung für Patentanmeldungen zur Gebrauchseignung und Entwicklung
mit Vollmacht

German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

daß mein Wohnsitz, meine Postanschrift und meine Staatsangehörigkeit den im nachstehenden nach meinem Namen aufgeführten Angaben entsprechen, daß ich nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent für die Erfindung mit folgendem Titel beantragt wird:
Schaltungsanordnung zum Bilden des Abschlusses einer analogen Teilnehmerleitung

deren Beschreibung hier beigefügt ist, es sei denn (in diesem Falle Zutreffendes bitte ankreuzen), diese Erfindung

☒ wurde angemeldet am January 5, 2000
unter der US-Anmeldenummer 09/807,993
und wurde am May 3, 2001 abgeändert (falls zutreffend)
oder

☐ unter der PCT internationalen Anmeldungsnummer
PCT/DE00/00046
und wurde am _____ abgeändert (falls zutreffend).

Ich bestätige hiermit, daß ich den Inhalt der oben angegebene Patentanmeldung, einschließlich der Ansprüche, die eventuell durch einen oben erwähnten Zusatzantrag abgeändert wurde, durchgesehen und verstanden habe.

Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 von Belang sind.

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäß Title 35, US-Code, § 119 (a)-(d), bzw. § 365(b) aller unten aufgeführten Auslandsanmeldungen für Patente oder Erfinderurkunden, oder § 365(a) aller PCT internationalen Anmeldungen, welche wenigstens ein Land ausser den Vereingten Staaten von Amerika benennen, und habe nachstehend durch ankreuzen sämtliche Auslandsanmeldungen für Patente bzw. Erfinderurkunden oder PCT internationale Anmeldungen angegeben, deren Anmeldetag dem der Anmeldung, für welche Priorität beansprucht wird, vorangeht.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Circuit Arrangement for Forming the Termination of an Analog Subscriber Line

the specification of which is attached hereto unless the following box is checked:

☒ was filed on January 5, 2000 as
United States Application Number 09/807,993
and was amended on May 3, 2001 (if applicable)
or,

☐ PCT International Application Number PCT/DE00/00046
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority under Title 35, United States Code §119 (a-d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States, listed below. I have also identified below, by checking the "No" box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is

Prior Foreign Applications
Frühere ausländische Anmeldungen

PriorityClaimed
Prioritätsanspruch

(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	☒ Yes Ja	☐ No Nein
199 01 464. 7	Germany	15/January/1999		
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	☐ Yes Ja	☐ No Nein

☐ Zusätzliche einstweilige Anmeldungsnummern sind im Prioritätsanhang aufgeführt.

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto.

German ... guage Utility or Design Patent Application ... aration

Ich beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)
(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)
(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)

☐ Zusätzliche einstweilige Anmeldungsnummern sind im ergänzenden Prioritätsanhang aufgeführt.

☐ Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

Ich beanspruche hiermit die mir unter Title 35, US-Code, § 120 zustehenden Vorteile aller unten aufgeführten US-Patentanmeldungen bzw. § 365(c) aller PCT internationalen Anmeldungen, welche die Vereinigten Staaten von Amerika benennen, und erkenne, insofern der Gegenstand eines jeden früheren Anspruchs dieser Patentanmeldung nicht in einer US-Patentanmeldung, bzw. PCT internationalen Anmeldung in in einer gemäß dem ersten Absatz von Title 35, US-Code, § 112 vorgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Title 37, Code of Federal Regulations, § 1.56 von Belang sind und die im Zeitraum zwischen dem Anmeldetag der früheren Patentanmeldung und dem nationalen oder im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesen (PCT) gültigen internationalen Anmeldetags bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application No.) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	(Status) (patentiert, schwebend, aufgegeben) (patented, pending, abandoned)
(Application No.) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	(Status) (patentiert, schwebend, aufgegeben) (patented, pending, abandoned)

☐ Zusätzliche USA oder internationale Anmeldungsnummern sind im ergänzenden Prioritätsanhang aufgeführt.

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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German Language Utility or Design Patent Application Declaration

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